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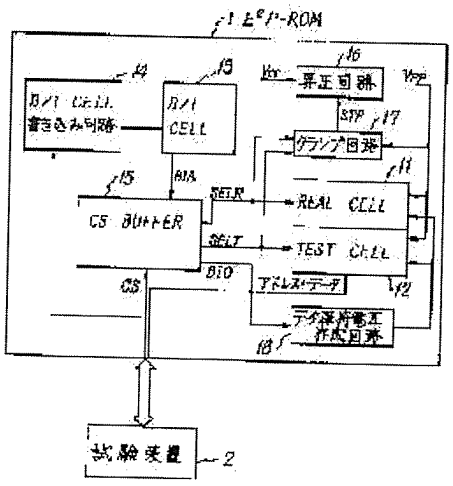
(54) NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND ITS TEST METHOD

(57)Abstract:

PURPOSE: To shorten test time, to enable a one hundred percent test and to improve reliability by applying a severe stress to the inside of a cell according to the real use conditions.

CONSTITUTION: A burn-in cell 13 is accessed from the outside and set to a normal or a test mode. When it is set to the normal mode, the access to the writing, deletion, reading of data against the memory device is performed only to a real cell 11. At the test mode setting, the access of the writing, deletion, and reading the data against the memory device is performed to a test cell 12. The voltage applied to the accessed cell becomes higher than that of the normal mode by a rewriting voltage pressure rising means 16 and a clamp 17. At the time of a test mode, a CG voltage pressure rising means 18 applies voltage higher than the normal mode to the control gate of each cell when there is no access of the writing, deletion, and reading of data.



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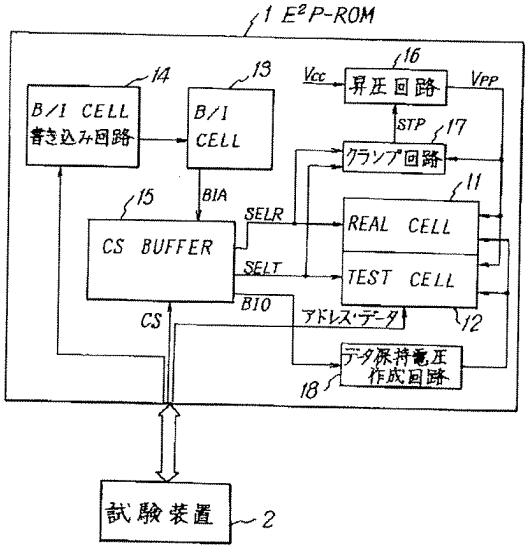
(54)【発明の名称】　不揮発性半導体記憶装置およびその試験方法

(57)【要約】

【目的】　電気的にデータの書き込みおよび消去がなされる不揮発性半導体装置およびその試験方法に関し、保証試験に要する時間を短縮し、しかも信頼性を向上させることを目的とする。

【構成】　外部からの設定により装置内を通常モードと試験モードに切り換え、切り換えたモード状態を保持するバーンインセルと、前記通常モードの時にのみアクセスがなされるリアルセルと、前記試験モードの時にのみアクセスがなされるテストセルと、前記試験モードの時に、データの書き込みまたは消去用の電圧を通常モードの時よりも高くする書換え電圧昇圧手段（１６、１７）と、前記試験モードの時に、アクセスのない時にセルのコントロールゲートに通常モードの時よりも高い電圧を印加するＣＧ電圧昇圧手段（１８）とを備えるように構成する。

本発明の一実施例の概略構成図



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【特許請求の範囲】

【請求項１】　電気的にデータの書き込みおよび消去がなされる不揮発性半導体記憶装置において、外部からの設定により装置内を通常モードと試験モードに切り換え、切り換えたモード状態を保持するバーンインセル（１３）と、前記通常モードの時にのみアクセスがなされるリアルセル（１１）と、前記試験モードの時にのみアクセスがなされるテストセル（１２）と、前記試験モードの時に、データの書き込みまたは消去用の電圧を通常モードの時よりも高くする書換え電圧昇圧手段（１６、１７）と、前記試験モードの時に、アクセスのない時にセルのコントロールゲートに通常モードの時よりも高い電圧を印加するＣＧ電圧昇圧手段（１８）と、を備えたことを特徴とする不揮発性半導体記憶装置。

【請求項２】　請求項１記載の不揮発性半導体記憶装置の試験方法であって、前記不揮発性半導体記憶装置を高温環境下に置き、前記バーンインセル（１３）を試験モードに設定して、前記テストセル（１２）へのデータの書き込みおよび消去を、前記書換え電圧昇圧手段（１６、１７）により通常モード時よりも高い電圧で行なうようにし、前記テストセル（１２）へのデータの書き込みおよび消去のアクセスを、所定回数繰り返し、そのアクセス終了後に書き込みデータの読み出し、照合を行なって判定することを特徴とする不揮発性半導体記憶装置の試験方法。

【請求項３】　請求項１記載の不揮発性半導体記憶装置の試験方法であって、前記不揮発性半導体記憶装置を高温環境下に置き、前記バーンインセル（１３）を通常モードに設定して、前記リアルセル（１１）に所定のデータの書き込みを行い、次に、前記バーンインセル（１３）を試験モードに設定して、前記テストセル（１２）に所定のデータの書き込みを行い、その後、アクセスを行なわずに、前記ＣＧ電圧昇圧手段（１８）によりセルのコントロールゲートに通常モード時よりも高い電圧が印加された状態で、所定時間放置し、その所定時間経過後に前記テストセル（１２）およびリアルセル（１１）から書き込みデータを読み出し、照合を行なって判定する、ことを特徴とする不揮発性半導体記憶装置の試験方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、電気的にデータの書き込みおよび消去がなされる不揮発性半導体記憶装置およびその試験方法に関する。

【０００２】電気的にデータの書き込みおよび消去がなされる不揮発性半導体記憶装置（以下、「E^2 Ｐ－ＲＯＭ」という）の特性においては、書換え回数に対する保証が大きな問題である。すなわち、カタログ上の書換え回数の値を保証しようとした場合には、メーカー側においては、その何倍もの書き換えをして、その上で不良の

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発生がないことを確認しなければならない。さらにE^2 Ｐ－ＲＯＭの特性においては、データ保証特性も問題になってくる。これはデータを書き込んだ後にそのデータをどれだけの期間保持できるかを保証するもので、仕様上では年単位の保証となっていて、メーカー側はこれに対する試験による保証も重要となっている。

【０００３】

【従来の技術】周知のように、ＦＬＯＴＯＸ（Floating Gate Tunnel Oxide）型のE^2 Ｐ－ＲＯＭに構成されるセルには、フローティングゲートが構成され、そのフローティングゲートの一部分に非常に薄い酸化膜の領域（トンネル部）があり、そこを介して電流を流し、フローティングゲートへの電子注入またはフローティングゲートからの電子放出を行うことにより、データの消去または書き込みがおこなわれる。このセルにはコントロールゲート、セレクトゲート、ソース電極、およびドレイン電極が形成されていて、セレクトゲートとドレイン電極に２０Ｖの電圧を印加することにより、データの書き込みとなるフローティングゲートからの電子放出がなされ、コントロールゲートとセレクトゲートに２０Ｖの電圧を印加することにより、データの消去となるフローティングゲートへの電子の注入がなされる。２０Ｖの電圧は、装置内部に電源電圧を昇圧する昇圧回路を備え、データの書き込みまたは消去の際にその昇圧回路から作成されている。

【０００４】このようなE^2 Ｐ－ＲＯＭに対して、従来における書換え回数保証試験は、高温環境下において高温によるストレスを与えた状態で、書き込みおよび消去の書き換え動作を数万回単位で繰り返すことにより行なっていた。また、データ保持特性の保証試験は、同じく高温環境下でストレスを与え、かつ通電状態にして一定期間放置することにより行なっていた。また、従来の試験では、装置内部を試験モードにするために、外部の試験装置からあらかじめ決められた端子に通常使用する電圧（例えば５Ｖ）よりも高い電圧（例えば１５Ｖ）が、試験モードにする間に加えられていた。

【０００５】

【発明が解決しようとする課題】しかしながら、上記従来のE^2 Ｐ－ＲＯＭの書換え回数の保証試験では、書換え回数の保証値の何倍もの書き換えを行なっているため、試験にはかなりの時間が必要となっていた。また、データ保持特性の保証試験でも、保証期間が１０年程にもなるため、高温下でストレスを与えた状態とはいえ、放置する試験期間もかなり長いものとなっていた。

【０００６】このように従来の保証試験にともなう時間と工数は多大で、結果的に製品の価格に影響し、テストコストの点から課題となっていた。また、保証試験は製品を使用して行われることから、当然従来では抜き取り試験となり、全数に対する保証とはならないため、信頼性の点においても課題となっていた。

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【０００７】本発明は、このような課題に鑑みて創案されたもので、保証試験に要する時間を短縮し、しかも信頼性を向上させることのできる不揮発性半導体記憶装置およびその試験方法を提供することを目的とする。

【０００８】

【課題を解決するための手段】上記目的を達成するため請求項１の本発明は、電気的にデータの書き込みおよび消去がなされる不揮発性半導体記憶装置において、外部からの設定により装置内を通常モードと試験モードに切り換え、切り換えたモード状態を保持するバーンインセルと、前記通常モードの時にのみアクセスされるリアルセルと、前記試験モードの時にのみアクセスされるテストセルと、前記試験モードの時に、データの書き込みまたは消去用の電圧を通常モードの時よりも高くする書換え電圧昇圧手段と、前記試験モードの時に、アクセスのない時にセルのコントロールゲートに通常モードの時よりも高い電圧を印加するＣＧ電圧昇圧手段とを備えるように構成する。

【０００９】請求項２の本発明は、前記請求項１記載の不揮発性半導体記憶装置の試験方法であって、前記不揮発性半導体記憶装置を高温環境下に置き、前記バーンインセルを試験モードに設定して、前記テストセルへのデータの書き込みおよび消去を、前記書換え電圧昇圧手段により通常モード時よりも高い電圧で行なうようにし、前記テストセルへのデータの書き込みおよび消去のアクセスを、所定回数繰り返し、そのアクセス終了後に書き込みデータの読み出し、照合を行なって判定するように構成する。

【００１０】請求項３の本発明は、前記請求項１記載の不揮発性半導体記憶装置の試験方法であって、前記不揮発性半導体記憶装置を高温環境下に置き、前記バーンインセルを通常モードに設定して、前記リアルセルに所定のデータの書き込みを行い、次に、前記バーンインセルを試験モードに設定して、前記テストセルに所定のデータの書き込みを行い、その後、アクセスを行なわずに、前記ＣＧ電圧昇圧手段によりセルのコントロールゲートに通常モード時よりも高い電圧が印加された状態で、所定時間放置し、その所定時間経過後に前記テストセルおよびリアルセルから書き込みデータを読み出し、照合を行なって判定するように構成する。

【００１１】

【作用】請求項１の本発明である不揮発性半導体記憶装置では、外部からバーンインセルにアクセスがなされ、通常モードまたは試験モードに設定される。通常モードに設定された時には、記憶装置に対するデータの書き込み、消去、読み出しのアクセスはリアルセルに対してのみなされる。試験モードに設定された時には、記憶装置に対するデータの書き込み、消去、読み出しのアクセスはテストセルに対してのみなされ、そしてそのデータの書き込みおよび消去においてアクセスされたセルに印加される電圧は、書換え電圧昇圧手段により通常モード時よりも高い電圧にされる。また、試験モードの時には、データの書き込み、消去、読み出しのアクセスのない時に、ＣＧ電圧昇圧手段により各セルのコントロールゲートには通常モード時よりも高い電圧が印加される。

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【００１２】請求項２の本発明の試験方法では、高温環境下に置いてストレスを与えるとともに、バーンインセルにアクセスして試験モードに設定し、データの書き込みおよび消去のアクセスを繰り返す。このときのアクセスされるテストセルには、書換え電圧昇圧手段によりデータの書き込みおよび消去のための電圧が通常モード時よりも高い電圧で印加されるため、より厳しいストレスが与えられてのデータ書換え保証試験となる。

【００１３】請求項２の本発明の試験方法では、高温環境下に置いてストレスを与えるとともに、リアルセル、テストセルともに所定のデータの書き込みを行った後に、試験モードに設定し、アクセスをしないで所定の時間放置する。このときの全セルには、ＣＧ電圧昇圧手段によりコントロールゲートに通常モード時よりも高い電圧が印加されるため、データ保持が不安定な状態にされてのデータ保持保証試験となる。

【００１４】

【実施例】以下、図面を参照して、本発明の実施例を詳細に説明する。図１は、本発明の不揮発性半導体記憶装置（E^2 Ｐ－ＲＯＭ）の一実施例の概略構成図である。同図において、１はE^2 Ｐ－ＲＯＭ、２は試験装置である。E^2 Ｐ－ＲＯＭ１において、１１は通常モード時にデータ記憶用としてアクセスされるリアルセル（REAL CELL）、１２は試験モード時のみアクセスがなされるテストセル（TEST CELL）、１３はバーンインセル（B/I CELL）であり、データが書き込まれたときにバーンインアクティブ（ＢＩＡ）信号をオンにし、装置内を試験モードに切り換えてその状態を保持し、消去されたときにはＢＩＡ信号をオフにして装置内を通常モードにしてその状態を保持する。１４はそのバーンインセル１３への書き込み回路であり、外部からのバーンインセル書き込み信号によりバーンインセル１３への書き込みを行ない、バーンインセル消去信号によりバーンインセル１３の消去を行なう。１５はチップセレクトバッファ（CS BUFFER）であり、外部からE^2 Ｐ－ＲＯＭ１へのアクセス信号であるチップセレクト（ＣＳ）信号とバーンインセル１３から出力されるＢＩＡ信号を入力し、両信号の論理によりリアルセル１１をセレクトするＳＥＬＲ信号、テストセル１２をセレクトするＳＥＬＴ信号、後述するデータ保持電圧作成回路１８を制御するＢＩＯ信号を出力する。１６および１７は、本発明の書換え電圧昇圧手段である。１６は昇圧回路であり、外部からのリアルセル１１またはテストセル１２への書き込みまたは消去時のアクセスにより作動して、書き込みまたは消去に必要な書換え電圧Ｖppを電源電圧Ｖccを昇圧して作成

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し、リアルセル１１またはテストセル１２へ供給する。１７はクランプ回路であり、昇圧回路１６から出力された書き換え電圧Vppを監視し、所定の電圧を超えた時に昇圧回路１６へのＳＴＰ信号をオンにし、所定の電圧まで下降した時にオフにする。本実施例ではチップセレクトバッファ１５から出力されるＳＥＬＲ信号とＳＥＬＴ信号が入力され、それらの信号により監視する所定の電圧値が異なるようにされている。昇圧回路１６ではクランプ回路１７からの信号ＳＴＰがオンになると、その信号ＳＴＰがオフになるまで昇圧を停止する。１８は本発明のＣＧ電圧昇圧手段であるデータ保持電圧作成回路であり、チップセレクトバッファ１５からのＢＩ０信号がオンになると、リアルセル１１およびテストセル１２の各セルのコントロールゲートへデータ保持電圧を出力する。

【００１５】図２は、上記構成におけるリアルセル１１とテストセル１２の選択に関する詳細な回路図である。同図（ａ）において、WL_0 ～WL_m はアドレスラインからデコードされたワードラインである。BL_1 ～BL_n はリアルセルアレイ１１ａのビットラインであり、BLT_1 ～BLT_1 はテストセルアレイ１２ａのビットラインである。それぞれのビットラインにはトランジスタが介挿されていて、それぞれのトランジスタへの制御信号Y_1 ～Y_n 、YT_1～YT_1 へは、アドレスラインのデコード信号が入力され、いずれかがオンにされることにより、ビットラインのうちの１つが選択されるようになされている。

【００１６】同図（ｂ）はビットラインデコーダの回路図である。ビットラインデコーダ２０にはチップセレクトバッファ１５から出力されるＳＥＬＲ信号とＳＥＬＴ信号とビットラインを選択するアドレスラインAD_0 ～AD_x が入力されている。同図に示すように、本実施例では、２つのデコーダ２０ａ、２０ｂが構成されている。一方のデコーダ２０ａには、ＳＥＬＲ信号とアドレスラインAD_0 ～AD_x が入力されてデコードされ、前記トランジスタへの制御信号Y_1 ～Y_n を出力するようになされ、他方のデコーダ２０ｂには、ＳＥＬＴ信号とアドレスラインAD_0 ～AD_x が入力されてデコードされ、前記トランジスタへの制御信号YT_1 ～YT_1 を出力するようになされている。すなわち、ＳＥＬＲ信号がオンの時には制御信号Y_1 ～Y_nが出力されてリアルセルアレイ１１ａのいずれかのビットラインが選択されるようにされ、ＳＥＬＴ信号がオンの時には制御信号YT_1 ～YT_1 が出力されてテストセルアレイ１２ａのいずれかのビットラインが選択されるようになされている。

【００１７】図３は、図１に示したクランプ回路１７の詳細な回路図である。クランプ回路はソースとゲートをショートさせて定電流負荷としたＭＯＳトランジスタを直列に接続して、その接続するトランジスタの数により、あらかじめ定めた電圧値を監視してその電圧値を超

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えた時にＳＴＰ信号を出力するようにしたものである。同図に示すように、本実施例では、２つのクランプ回路１７ａ、１７ｂとＯＲ回路１７ｃが構成され、それぞれのクランプ回路１７ａ、１７ｂには昇圧回路１６の出力する書換え電圧Vppが入力される。一方のクランプ回路１７ａには、定電流負荷としたＭＯＳトランジスタがａ個接続され、その最終段に制御用のトランジスタT_1 が介挿され、そのゲートに制御信号としてＳＥＬＲ信号が入力されている。他方のクランプ回路１７ｂには、定電流負荷としたＭＯＳトランジスタがｂ個接続され、その最終段に制御用のトランジスタT_2 が介挿され、そのゲートに制御信号としてＳＥＬＴ信号が入力されている。そして、それぞれのクランプ回路１７ａ、１７ｂの出力はＯＲ回路１７ｃを介してＳＴＰ信号として出力されるようになされている。すなわち、チップセレクトバッファ１５からＳＥＬＲ信号が出力された場合には、クランプ回路１７ａが作動して設定されている書換え電圧を監視してＳＴＰ信号を出力し、チップセレクトバッファ１５からＳＥＬＴ信号が出力された場合には、クランプ回路１７ｂが作動して設定されている書換え電圧を監視してＳＴＰ信号を出力するように構成されている。

【００１８】図４は、図１に示したデータ保持電圧作成回路１８の詳細図である。同図に示すように、データ保持電圧作成回路１８は、ゲートにＢＩ０信号を入力したトランジスタT_3 により電源電圧V_{cc}を出力制御するものである。すなわち、チップセレクトバッファ１５からＢＩ０信号が出力されると、トランジスタT_3 がオンして電源電圧V_{cc}が出力される。その電源電圧V_{cc}はリアルセル１１およびテストセル１２の各セルのコントロールゲート（ＣＧ）へ印加されるようになされている。

【００１９】図５は、本実施例のE^2 Ｐ－ＲＯＭの信号論理と動作の説明図である。本実施例のE^2 Ｐ－ＲＯＭでは、図１に示したように、外部からバーンインセル書き込み回路１４を介してバーンインセル１３に書き込みがあると、バーンインセル１３はＢＩＡ信号を発して装置内部を試験モードにする。すなわち、図５に示すように、ＢＩＡ信号が論理“Ｈ”になった時が試験モードとなり、この状態で、アクセス信号として論理“Ｈ”のチップセレクト（ＣＳ）信号が入力された時には、チップセレクトバッファ１５はＳＥＬＴ信号をオンにする。これによりテストセル１２のみが選択されることになり、外部からの書き込み、消去、読み出しに係わるアクセスは、図２において説明したように、テストセルアレイ１２ａのうちのいずれかのセルがアクセスされ、リアルセルアレイ１１ａはアクセスされない。また、この状態では図３に示したように、クランプ回路１７ｂに設定されている監視電圧により、昇圧回路１６において昇圧される書換え電圧が決まり、その書換え電圧が書き込みまたは消去のときにテストセル１２に供給される。

【００２０】そして、ＢＩＡ信号が論理“Ｈ”の時に、

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ＣＳ信号が論理“Ｌ”にされると、チップセレクトバッファ１５はＢＩ０信号をオンにする。これにより、データ保持電圧作成回路１８が作動し、リアルセル１１とテストセル１２の全てのセルのコントロールゲートに電源電圧Ｖccが印加されることになる。

【００２１】一方、バーンインセル１３が消去されてＢＩＡ信号が論理“Ｌ”にされた時には、ＣＳ信号が論理“Ｈ”でリアルセル１１がスタンバイの状態となり、ＣＳ信号が論理“Ｌ”にされると、チップセレクトバッファ１５はＳＥＬＲ信号をオンにする。これによりリアルセル１１のみが選択され、外部からの書き込み、消去、読み出しに係わるアクセスは、図２において説明したように、リアルセルアレイ１１ａのうちのいずれかのセルがアクセスされ、テストセルアレイ１２ａはアクセスされない。また、この状態では図３に示したように、クランプ回路１７ｂに設定されている監視電圧値により、昇圧回路１６において昇圧される書換え電圧が決まり、その書換え電圧が書き込みまたは削除のときにリアルセル１１に供給される。

【００２２】次に、本実施例のE² Ｐ－ＲＯＭの特性保証試験を説明する。図６は、本実施例のE² Ｐ－ＲＯＭの通常時と試験時の条件表である。同表に示す条件におけるE² Ｐ－ＲＯＭは、図３に示したクランプ回路１７ａが２０Ｖ、クランプ回路１７ｂが２５Ｖの監視電圧に設定され、データ保持電圧作成回路１８のＶccは７Ｖに設定される。特性保証試験は、１５０°Ｃの温度環境下にE² Ｐ－ＲＯＭを置き、書換え回数保証試験とデータ保持保証試験について行われる。書換え回数保証試験は、試験装置２が、まずE² Ｐ－ＲＯＭ１のバーンインセル書き込み回路１４にアクセスしてバーンインセル１３に書き込みを行い、ＢＩＡ信号を“Ｈ”にして装置内を試験モードに設定し、次にＣＳ信号を論理“Ｈ”にする。そしてテストセル１２の各セルを順次アクセスしてデータを書き込み、消去を行う。このデータの書き込み、消去を所定回数繰り返す。このときのデータ書き込み消去は、その書き込み消去に伴うゲートへの電圧印加が通常時の２０Ｖと異なり２５Ｖが印加され、実使用条件よりも厳しいストレスが与えられて行なわれる。所定回数の書き込み、消去が終了するとテストセル１２の各セルに対して正常に書き込み、消去がなされるかどうかをチェックする。正常であれば、次にデータ保持保証試験が行われる。データ保持保証試験は、ＣＳ信号を論理“Ｌ”にしてリアルセル１１とテストセル１２の全てのセルのコントロールゲートに７Ｖを印加して、データ保持を不安定にした状態で所定の時間放置する。所定時間の経過後にデータの読み出しを行い、書き込みデータとの照合を行ってデータの保持をチェックする。

【００２３】このように、本実施例では、書換え回数保証試験においては、通常の書き込みおよび消去に使われる２０Ｖの電圧よりも、さらに高電圧な２５Ｖの電圧で

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書き込みおよび消去が行なわれ、セルに実使用条件よりも厳しいストレスを与えての試験となるため、従来よりも少ない書換え回数で保証試験が達成でき、試験時間が短縮される。また、データ保持保証試験においては、通常時のデータ保持状態のときにコントロールゲートへ印加されている電圧よりもの高い電圧が印加され、データ保持状態が不安定になる電圧状態にされての試験となるため、従来よりも短い放置時間で保証試験が達成でき、試験時間が短縮される。

【００２４】また、本実施例の試験は、E² Ｐ－ＲＯＭにテストの時のみ使用するテストセルを設けて行われるため、全数に対する試験が実施でき、特性保証の信頼性が向上する。

【００２５】さらに、本実施例のE² Ｐ－ＲＯＭには、装置内部を試験モードにするバーンインセルを設けているため、試験装置において特別な電圧を作成する必要がなく、また試験モードにある間に特別な電圧をE² Ｐ－ＲＯＭに入力しておく必要もなく、試験装置の負担を軽減するものとなっている。

【００２６】

【発明の効果】以上説明したように、本発明では、セルに実使用条件より厳しいストレスを内部において加えることにより時間的により加速された特性保証試験としているため、試験時間を短縮する効果が大である。また、テストセルを設けたことにより全数試験が可能になるため、信頼性を向上させることができる。

【図面の簡単な説明】

【図１】本発明のE² Ｐ－ＲＯＭの一実施例の概略構成図である。

【図２】実施例におけるリアルセルとテストセルのセレクトに関する詳細な回路図である。

【図３】実施例のクランプ回路の詳細な回路図である。

【図４】実施例のデータ保持電圧作成回路の詳細図である。

【図５】本実施例におけるE² Ｐ－ＲＯＭの信号論理と動作の説明図である。

【図６】本実施例のE² Ｐ－ＲＯＭの通常時と試験時の条件表である。

【符号の説明】

１…E² Ｐ－ＲＯＭ
２…試験装置
１１…リアルセル
１２…テストセル
１３…バーンインセル
１４…バーンインセル書き込み回路
１５…チップセレクトバッファ回路
１６…昇圧回路
１７、１７ａ、１７ｂ…クランプ回路
１８…データ保持電圧作成回路
１１ａ…リアルラインアレイ

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１２ａ…テストラインアレイ
ＷＬ…ワードライン

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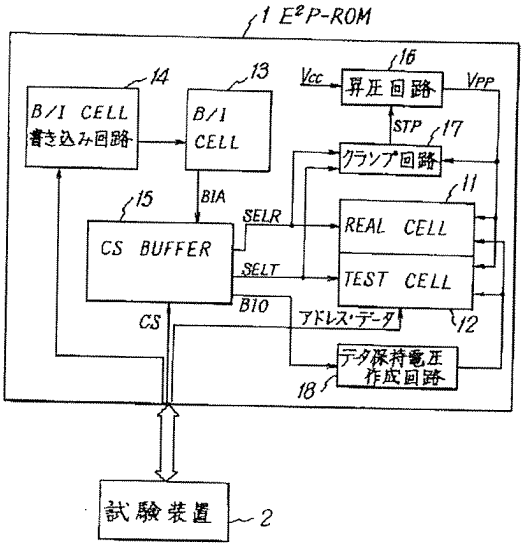
ＢＬ…ビットライン
２０、２０ａ、２０ｂ…ビットラインデコーダ

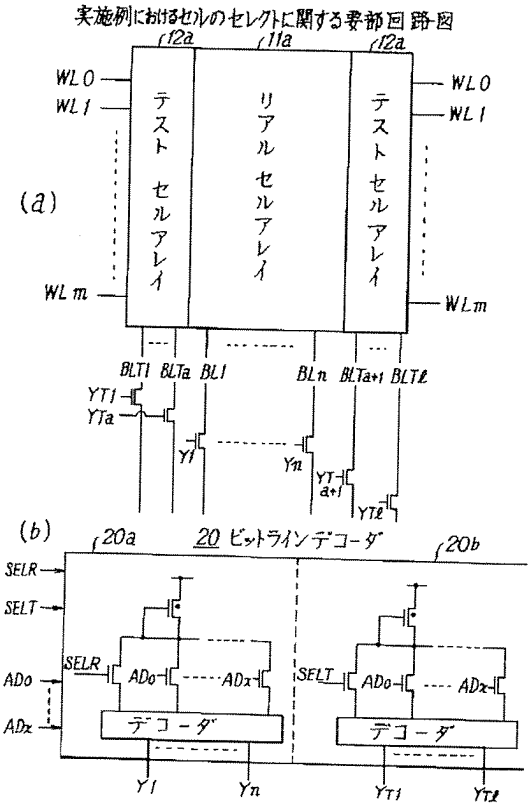
【図１】

本発明の一実施例の概略構成図



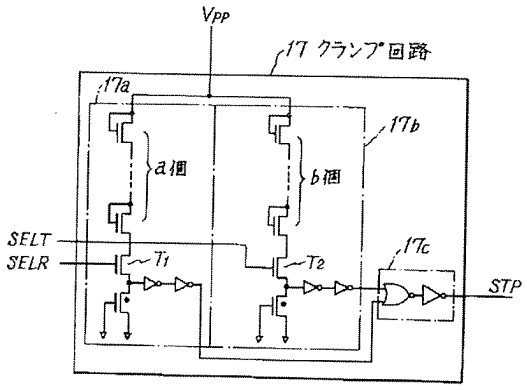
【図２】

実施例におけるセルのセレクトに関する要部回路図



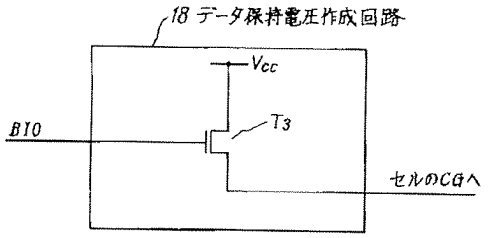
【図３】

本実施例のクランプ回路の詳細な回路図



【図４】

本実施例のデータ保持電圧作成回路の詳細図



【図5】

本実施例におけるE^2P-ROMの信号論理と動作の説明図

BIA信号	CS信号	動作
H	H	TEST CELL 選択 (SELT信号オン)
	L	TEST & REAL CELL 選択 (EEPROM CGにVcc) (BIO信号オン)
L	H	REAL CELL 選択 (スタンバイ)
	L	REAL CELL 選択 (アクティブ) (SELR信号オン)

【図6】

実施例の通常時と試験時の条件表

	通常時	試験時
書込み消去電圧 (VPP)	～20V	～25V
データ保持の時のコントロールゲート電圧	0～2V	～7V
温度環境	0～70°C	150°C

PATENT ABSTRACTS OF JAPAN

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FUJITSU VLSI LTD

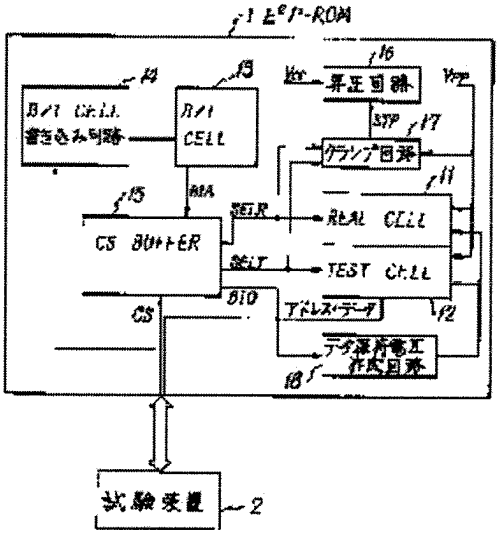
(72)Inventor : TSUJIMURA YOSHINORI

(54) NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND ITS TEST METHOD

(57)Abstract:

PURPOSE: To shorten test time, to enable a one hundred percent test and to improve reliability by applying a severe stress to the inside of a cell according to the real use conditions.

CONSTITUTION: A burn-in cell 13 is accessed from the outside and set to a normal or a test mode. When it is set to the normal mode, the access to the writing, deletion, reading of data against the memory device is performed only to a real cell 11. At the test mode setting, the access of the writing, deletion, and reading the data against the memory device is performed to a test cell 12. The voltage applied to the accessed cell becomes higher than that of the normal mode by a rewriting voltage pressure rising means 16 and a clamp 17. At the time of a test mode, a CG voltage pressure rising means 18 applies voltage higher than the normal mode to the control gate of each cell when there is no access of the writing, deletion, and reading of data.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the non-volatile semiconductor memory with which the writing and elimination of data are made electrically, and its test method.
[0002] In the property of a non-volatile semiconductor memory (henceforth "E2 P-ROM") that the writing and elimination of data are made electrically, the guarantee to the count of rewriting is a big problem. That is, when it is going to guarantee the value of the count of rewriting on a catalog, it must check that the numbers of times as many rewriting as this is turned on a manufacturer side, and there is no generating of a defect on it. Furthermore in the property of E2 P-ROM, a data guarantee property also becomes a problem. This guarantees which after writing in data, can carry out period maintenance of the data, serves as a guarantee of a year unit on the specification, and the guarantee by the trial to this is also important for a manufacturer side.
[0003]
[Description of the Prior Art] As everyone knows, the floating gate is constituted by the cel constituted by E2 P-ROM of a FLOTOX (Floating Gate Tunnel Oxide) mold, there is a field (tunnel section) of a very thin oxide film in it in a part of the floating gate, and elimination or the writing of data is performed in a current through there by performing electron emission from the electron injection or the floating gate to a sink and the floating gate. By forming the control gate, the selection gate, the source electrode, and the drain electrode in this cel, and impressing the electrical potential difference of 20V to the selection gate and a drain electrode, the electron emission from the floating gate used as the writing of data is made, and impregnation of the electron to the floating gate used as elimination of data is made by impressing the electrical potential difference of 20V to the control gate and the selection gate. The electrical potential difference of 20V equips the interior of equipment with the booster circuit which carries out pressure up of the supply voltage, and is created from the booster circuit in the case of the writing of data, or elimination.
[0004] the condition which the count guarantee test of rewriting in the former gave the stress by the elevated temperature in the bottom of hot environments to such E2 P-ROM -- it is -- writing and rewriting actuation of elimination -- tens of thousands of times unit -- winding -- ****** -- things were performing. Moreover, similarly the guarantee test of a data-hold property gave stress under hot environments, and it was changed into the energization condition and it was performing it by carrying out fixed period neglect. Moreover, in the conventional trial, in order to make the interior of equipment into test mode, the electrical potential difference (for example, 15V) higher than the electrical potential difference (for example, 5V) usually used for the terminal beforehand decided from the external testing device was applied, while making it test mode.
[0005]
[Problem(s) to be Solved by the Invention] However, in the guarantee test of the count of rewriting of above-mentioned conventional E2 P-ROM, since numbers of times as much rewriting as the certified value of the count of rewriting was performed, most time amount was needed for the trial. Moreover, the duration of test which also leaves the guarantee test of a data-hold property although it is the condition which gave stress under the elevated temperature since the term of a guarantee becomes about ten years also became quite long.
[0006] Thus, the conventional time amount and the manday accompanying a guarantee test were great, influenced the price of a product as a result, and had become a technical problem from the point of test cost. Moreover, since it became a sampling test in the former and the guarantee to total naturally did not consist of being carried out using a product, the guarantee test had become a technical problem also in the point of dependability.
[0007] It was originated in view of such a technical problem, and this invention shortens the time amount which a guarantee test takes, and aims at offering the non-volatile semiconductor memory which can moreover raise

dependability, and its test method.
[0008]
[Means for Solving the Problem] In order to attain the above-mentioned object this invention of claim 1 In the non-volatile semiconductor memory with which the writing and elimination of data are made electrically The burn-in cel holding the mode condition which switched the inside of equipment to the normal mode and test mode, and was switched by setting out from the outside, The real cel accessed only at the time of said normal mode, and the test cell accessed only at the time of said test mode, The rewriting electrical-potential-difference pressure-up means which makes the writing of data, or the electrical potential difference for elimination higher than the time of the normal mode at the time of said test mode, When there is no access at the time of said test mode, it constitutes so that it may have a CG electrical-potential-difference pressure-up means to impress an electrical potential difference higher than the time of the normal mode to the control gate of a cel.
[0009] This invention of claim 2 is the test method of said non-volatile semiconductor memory according to claim 1, put said non-volatile semiconductor memory on the bottom of hot environments, and said burn-in cel is set as test mode. Said rewriting electrical-potential-difference pressure-up means is made to perform the writing and elimination of the data to said test cell on an electrical potential difference higher than the time of the normal mode. The writing of the data to said test cell and access of elimination are written in after the count repeat of predetermined, and its access termination, and it constitutes so that it may judge by performing read-out of data and collating.
[0010] This invention of claim 3 is the test method of said non-volatile semiconductor memory according to claim 1, put said non-volatile semiconductor memory on the bottom of hot environments, and said burn-in cel is set as the normal mode. Write predetermined data in said real cel, next said burn-in cel is set as test mode. Without writing predetermined data in said test cell, and performing access after that, where an electrical potential difference higher than the time of the normal mode is impressed to the control gate of a cel by said CG electrical-potential-difference pressure-up means Predetermined time neglect is carried out, it writes in from said test cell and real cel after the predetermined time progress, and data are read, and it constitutes so that it may collate and judge.
[0011]
[Function] In the non-volatile semiconductor memory which is this invention of claim 1, access is made by the burn-in cel from the exterior, and it is set as the normal mode or test mode. When set as the normal mode, access of the writing of data to a store, elimination, and read-out is made only to a real cel. When set as test mode, access of the writing of data to a store, elimination, and read-out is made only to a test cell, and the electrical potential difference impressed to the cel accessed in the writing and elimination of the data is made into an electrical potential difference higher than the time of the normal mode by the rewriting electrical-potential-difference pressure-up means. Moreover, at the time of test mode, when there is no access of the writing of data, elimination, and read-out, an electrical potential difference higher than the time of the normal mode is impressed to the control gate of each cel by CG electrical-potential-difference pressure-up means.
[0012] In the test method of this invention of claim 2, while putting on the bottom of hot environments and giving stress, a burn-in cel is accessed, it is set as test mode, and the writing of data and access of elimination are repeated. Since the electrical potential difference for the writing of data and elimination is impressed on an electrical potential difference higher than the time of the normal mode by the rewriting electrical-potential-difference pressure-up means, it becomes a data rewriting guarantee test [that severer stress is given] at the test cell by which it is accessed at this time.

[0013] while putting on the bottom of hot environments and giving stress in the test method of this invention of claim 2, after a real cel and a test cell write in predetermined data, without it accesses by setting it as test mode -- predetermined time amount neglect -- it carries out. Since an electrical potential difference higher than the time of the normal mode is impressed to the control gate by CG electrical-potential-difference pressure-up means, data-hold becomes all the cels at this time with a data-hold guarantee test [changing into an unstable condition].
[0014]
[Example] Hereafter, the example of this invention is explained to a detail with reference to a drawing. Drawing 1 is the outline block diagram of one example of the non-volatile semiconductor memory (E2 P-ROM) of this invention. In this drawing, 1 is E2 P-ROM and 2 is a testing device. The real cel by which 11 is accessed as an object for data storage in E2 P-ROM1 at the time of the normal mode (REAL CELL), The test cell by which, as for 12, access is made only at the time of test mode (TEST CELL), 13 is a burn-in cel (B/I CELL), and when data are written in, a burn-in active (BIA) signal is turned ON. The inside of equipment is switched to test mode, the condition is held, when eliminated, a BIA signal is turned OFF, the inside of equipment is made into the normal mode, and the condition is held. 14 is a write-in circuit to the burn-in cel 13, performs the writing to the burn-in cel 13 with the burn-in cel write-

in signal from the outside, and eliminates the burn-in cel 13 with a burn-in cel elimination signal. 15 is a chip select buffer (CS BUFFER), inputs the chip select (CS) signal which is an access signal from the outside to E2 P-ROM1, and the BIA signal outputted from the burn-in cel 13, and outputs the SELR signal which selects the real cel 11 by the logic of both signals, the SELT signal which selects a test cell 12, and BI0 signal which controls the data-hold electrical-potential-difference creation circuit 18 mentioned later. 16 and 17 are the rewriting electrical-potential-difference pressure-up means of this invention. 16 is a booster circuit, it operates by the writing to the real cel 11 or test cell 12 from the outside, or access at the time of elimination, carries out pressure up of the supply voltage Vcc, creates the rewriting electrical potential difference Vpp required for writing or elimination, and supplies it to the real cel 11 or a test cell 12. It rewrites and an electrical potential difference Vpp is supervised, when [at which the predetermined electrical potential difference was exceeded] outputted from a booster circuit 16, it is a clamping circuit, 17 turns ON the STP signal to a booster circuit 16, and when it descends to a predetermined electrical potential difference, it turns it OFF. The SELR signal and SELT signal which are outputted from the chip select buffer 15 are inputted, and he is trying for the predetermined electrical-potential-difference values supervised with those signals to differ in this example. In a booster circuit 16, if the signal STP from a clamping circuit 17 is turned on, pressure up will be stopped until the signal STP becomes off. 18 is a data-hold electrical-potential-difference creation circuit which is CG electrical-potential-difference pressure-up means of this invention, and if BI0 signal from the chip select buffer 15 is turned on, it will output a data-hold electrical potential difference to the control gate of each cel of the real cel 11 and a test cell 12.

[0015] Drawing 2 is a detailed circuit diagram about selection of the real cel 11 in the above-mentioned configuration, and a test cell 12. It sets to this drawing (a) and is WL0 -WLm. It is the WORD line decoded from the address line. BL1 -BLn It is the bit line of real cel array 11a, and they are BLT1 - BLTl. It is the bit line of test-cell array 12a. a transistor inserts in each bit line -- having -- **** -- control signal Y1 -Yn to each transistor, and YT1-YTl **** -- the decoding signal of an address line is inputted and it is made as [choose / one of the bit lines] by turning either ON.

[0016] This drawing (b) is a circuit diagram of a bit-line decoder. Address line AD0 -ADx which chooses as the bit-line decoder 20 the SELR signal and SELT signal which are outputted from the chip select buffer 15, and the bit line It is inputted. As shown in this drawing, two decoders 20a and 20b consist of this examples. In one decoder 20a, they are a SELR signal and address line AD0 -ADx. It is inputted and decoded and is control signal Y1 -Yn to said transistor. It is made as [output] and they are a SELT signal and address line AD0 -ADx in decoder 20b of another side. It is inputted and decoded and is control signal YT1 -YTl to said transistor. It is made as [output]. That is, when control signal Y1 -Yn is outputted when a SELR signal is ON, and it is made to be chosen in one bit line of the real cel array 11a and a SELT signal is ON, it is control signal YT1 -YTl. It is made as [choose / it is outputted and / one bit line of the test-cell array 12a].

[0017] Drawing 3 is the detailed circuit diagram of the clamping circuit 17 shown in drawing 1 . A clamping circuit connects to a serial the MOS transistor which the source and the gate were made to short-circuit and was used as the constant current load, and when the electrical-potential-difference value defined beforehand is supervised and the electrical-potential-difference value is exceeded with the number of the transistors which connect, it is made to output an STP signal. As shown in this drawing, in this example, two clamping circuits 17a and 17b and OR circuit 17c are constituted, and the rewriting electrical potential difference Vpp which a booster circuit 16 outputs is inputted into each clamping circuit 17a and 17b. a MOS transistors used as the constant current load are connected to one clamping circuit 17a, and it is the transistor T1 for control to the last stage. It is inserted and the SELR signal is inputted into the gate as a control signal. b MOS transistors used as the constant current load are connected to clamping circuit 17b of another side, and it is the transistor T2 for control to the last stage. It is inserted and the SELT signal is inputted into the gate as a control signal. And the output of each clamping circuit 17a and 17b is made as [output / through OR circuit 17c / as an STP signal]. That is, when the rewriting electrical potential difference to which clamping circuit 17a operates and is set when a SELR signal is outputted from the chip select buffer 15 is supervised, an STP signal is outputted and a SELT signal is outputted from the chip select buffer 15, it is constituted so that the rewriting electrical potential difference to which clamping circuit 17b operates and is set may be supervised and an STP signal may be outputted.

[0018] Drawing 4 is the detail drawing of the data-hold electrical-potential-difference creation circuit 18 shown in drawing 1 . It is transistor T3 as which the data-hold electrical-potential-difference creation circuit 18 inputted BI0 signal into the gate as shown in this drawing. The output control of the supply voltage Vcc is carried out. That is, it is transistor T3 when BI0 signal is outputted from the chip select buffer 15. It turns on and supply voltage Vcc is outputted. The supply voltage Vcc is made as [impress / at the control gate (CG) of each cel of the real cel 11 and a test cell 12].

[0019] Drawing 5 is the signal logic of E2 P-ROM of this example, and an explanatory view of operation. In E2 P-

ROM of this example, if the burn-in cel 13 has writing through the burn-in cel write-in circuit 14 from the exterior as shown in drawing 1 , the burn-in cel 13 will emit a BIA signal, and will make the interior of equipment test mode. That is, as shown in drawing 5 , when the time of a BIA signal becoming logic"H" becomes test mode and the logic" chip select (CS) signal of H" is inputted as an access signal in this condition, the chip select buffer 15 turns ON a SELT signal. As only a test cell 12 will be chosen by this and access concerning the writing from the outside, elimination, and read-out was explained in drawing 2 , the cel of either of the test-cell array 12a is accessed, and real cel array 11a is not accessed. Moreover, in this condition, as shown in drawing 3 , the rewriting electrical potential difference pressure up is carried out [an electrical potential difference] in a booster circuit 16 by the monitor electrical potential difference set as clamping circuit 17b is decided, and when that rewriting electrical potential difference is writing or elimination, a test cell 12 is supplied.

[0020] And if CS signal is made into logic "L" when a BIA signal is logic"H", the chip select buffer 15 will turn ON BI0 signal. By this, the data-hold electrical-potential-difference creation circuit 18 will operate, and supply voltage Vcc will be impressed to the control gate of the real cel 11 and all the cels of a test cell 12.

[0021] If CS signal will be in the condition of standby of the real cel 11 by logic"H" and CS signal is made into logic "L" on the other hand when the burn-in cel 13 is eliminated and a BIA signal is made into logic "L", the chip select buffer 15 will turn ON a SELR signal. As only the real cel 11 was chosen by this and access concerning the writing from the outside, elimination, and read-out was explained in drawing 2 , the cel of either of the real cel array 11a is accessed, and test-cell array 12a is not accessed. Moreover, in this condition, as shown in drawing 3 , the rewriting electrical potential difference pressure up is carried out [an electrical potential difference] in a booster circuit 16 by the monitor electrical-potential-difference value set as clamping circuit 17b is decided, and when that rewriting electrical potential difference is writing or deletion, the real cel 11 is supplied.

[0022] Next, the property guarantee test of E2 P-ROM of this example is explained. Drawing 6 is a condition table at the time of usual [of E2 P-ROM of this example], and a trial. Clamping circuit 17a which showed E2 P-ROM in the conditions shown in this table to drawing 3 is set as the monitor electrical potential difference which is 25V for 20V and clamping circuit 17b, and Vcc of the data-hold electrical-potential-difference creation circuit 18 is set as 7V. A property guarantee test puts E2 P-ROM on the bottom of the temperature environment of 150-degreeC, and is performed about the count guarantee test of rewriting, and a data-hold guarantee test. A testing device 2 accesses the burn-in cel write-in circuit 14 of E2 P-ROM1 first, and writes in the burn-in cel 13, and the count guarantee test of rewriting makes a BIA signal "H", sets the inside of equipment as test mode, and then makes CS signal logic"H". And it eliminates by carrying out sequential access of each cel of a test cell 12, and writing in data. The writing of this data and elimination are repeated the number of predetermined times. Unlike 20V at the time, 25V are usually impressed for the electrical-potential-difference impression to the gate accompanying that write-in elimination, and data write-in elimination at this time is performed by giving stress severer than a real service condition. After the writing of the count of predetermined and elimination are completed, it writes in normally to each cel of a test cell 12, and it is confirmed whether elimination is made or not. If normal, a data-hold guarantee test will be performed next. time amount neglect predetermined in the condition of the data-hold guarantee test having made CS signal logic "L", and having impressed 7V to the control gate of the real cel 11 and all the cels of a test cell 12, and having made data-hold into instability -- it carries out. Data are read after progress of predetermined time, collating with write-in data is performed, and maintenance of data is checked.

[0023] Thus, in this example, in the count guarantee test of rewriting, writing and elimination are performed on the still high tension electrical potential difference of 25V, rather than the electrical potential difference of 20V used for usual writing and usual elimination, since it becomes the trial which gives stress severer than a real service condition to a cel, a guarantee test can be attained by the count of rewriting smaller than before, and test time is shortened. Moreover, in a data-hold guarantee test, an electrical potential difference higher than the electrical potential difference usually impressed in the data-hold condition at the time at the control gate is impressed, since it becomes the trial of changing into the electrical-potential-difference condition that a data-hold condition becomes instability, a guarantee test can be attained by neglect time amount shorter than before, and test time is shortened.

[0024] Moreover, since the trial of this example is performed to E2 P-ROM by preparing the test cell which uses it only at the time of a test, it can carry out the trial to total and its dependability of a property guarantee improves.

[0025] Furthermore, since the burn-in cel which makes the interior of equipment test mode is prepared in E2 P-ROM of this example, while not creating a special electrical potential difference in the testing device and being in test mode, a special electrical potential difference did not need to be inputted into E2 P-ROM, and the burden of a testing device has been mitigated.

[0026]

[Effect of the Invention] Since it is considering as the property guarantee test accelerated more in time by adding stress severer than a real service condition to a cel inside in this invention as explained above, the effectiveness of shortening test time is size. Moreover, since a 100% test becomes possible by having prepared the test cell, dependability can be raised.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, in the guarantee test of the count of rewriting of above-mentioned conventional E2 P-ROM, since numbers of times as much rewriting as the certified value of the count of rewriting was performed, most time amount was needed for the trial. Moreover, the duration of test which also leaves the guarantee test of a data-hold property although it is the condition which gave stress under the elevated temperature since the term of a guarantee becomes about ten years also became quite long.
[0006] Thus, the conventional time amount and the manday accompanying a guarantee test were great, influenced the price of a product as a result, and had become a technical problem from the point of test cost. Moreover, since it became a sampling test in the former and the guarantee to total naturally did not consist of being carried out using a product, the guarantee test had become a technical problem also in the point of dependability.
[0007] It was originated in view of such a technical problem, and this invention shortens the time amount which a guarantee test takes, and aims at offering the non-volatile semiconductor memory which can moreover raise dependability, and its test method.

[Translation done.]

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EXAMPLE

[Example] Hereafter, the example of this invention is explained to a detail with reference to a drawing. Drawing 1 is the outline block diagram of one example of the non-volatile semiconductor memory (E2 P-ROM) of this invention. In this drawing, 1 is E2 P-ROM and 2 is a testing device. The real cel by which 11 is accessed as an object for data storage in E2 P-ROM1 at the time of the normal mode (REAL CELL), The test cell by which, as for 12, access is made only at the time of test mode (TEST CELL), 13 is a burn-in cel (B/I CELL), and when data are written in, a burn-in active (BIA) signal is turned ON. The inside of equipment is switched to test mode, the condition is held, when eliminated, a BIA signal is turned OFF, the inside of equipment is made into the normal mode, and the condition is held. 14 is a write-in circuit to the burn-in cel 13, performs the writing to the burn-in cel 13 with the burn-in cel write-in signal from the outside, and eliminates the burn-in cel 13 with a burn-in cel elimination signal. 15 is a chip select buffer (CS BUFFER), inputs the chip select (CS) signal which is an access signal from the outside to E2 P-ROM1, and the BIA signal outputted from the burn-in cel 13, and outputs the SELR signal which selects the real cel 11 by the logic of both signals, the SELT signal which selects a test cell 12, and BI0 signal which controls the data-hold electrical-potential-difference creation circuit 18 mentioned later. 16 and 17 are the rewriting electrical-potential-difference pressure-up means of this invention. 16 is a booster circuit, it operates by the writing to the real cel 11 or test cell 12 from the outside, or access at the time of elimination, carries out pressure up of the supply voltage Vcc, creates the rewriting electrical potential difference Vpp required for writing or elimination, and supplies it to the real cel 11 or a test cell 12. It rewrites and an electrical potential difference Vpp is supervised, when [at which the predetermined electrical potential difference was exceeded] outputted from a booster circuit 16, it is a clamping circuit, 17 turns ON the STP signal to a booster circuit 16, and when it descends to a predetermined electrical potential difference, it turns it OFF. The SELR signal and SELT signal which are outputted from the chip select buffer 15 are inputted, and he is trying for the predetermined electrical-potential-difference values supervised with those signals to differ in this example. In a booster circuit 16, if the signal STP from a clamping circuit 17 is turned on, pressure up will be stopped until the signal STP becomes off. 18 is a data-hold electrical-potential-difference creation circuit which is CG electrical-potential-difference pressure-up means of this invention, and if BI0 signal from the chip select buffer 15 is turned on, it will output a data-hold electrical potential difference to the control gate of each cel of the real cel 11 and a test cell 12.

[0015] Drawing 2 is a detailed circuit diagram about selection of the real cel 11 in the above-mentioned configuration, and a test cell 12. It sets to this drawing (a) and is WL0 -WLm. It is the WORD line decoded from the address line. BL1 -BLn It is the bit line of real cel array 11a, and they are BLT1 - BLTl. It is the bit line of test-cell array 12a. a transistor inserts in each bit line -- having -- **** -- control signal Y1 -Yn to each transistor, and YT1-YTl **** -- the decoding signal of an address line is inputted and it is made as [choose / one of the bit lines] by turning either ON.

[0016] This drawing (b) is a circuit diagram of a bit-line decoder. Address line AD0 -ADx which chooses as the bit-line decoder 20 the SELR signal and SELT signal which are outputted from the chip select buffer 15, and the bit line It is inputted. As shown in this drawing, two decoders 20a and 20b consist of this examples. In one decoder 20a, they are a SELR signal and address line AD0 -ADx. It is inputted and decoded and is control signal Y1 -Yn to said transistor. It is made as [output] and they are a SELT signal and address line AD0 -ADx in decoder 20b of another side. It is inputted and decoded and is control signal YT1 -YTl to said transistor. It is made as [output]. That is, when control signal Y1 -Yn is outputted when a SELR signal is ON, and it is made to be chosen in one bit line of the real cel array 11a and a SELT signal is ON, it is control signal YT1 -YTl. It is made as [choose / it is outputted and / one bit line of the test-cell array 12a].

[0017] Drawing 3 is the detailed circuit diagram of the clamping circuit 17 shown in drawing 1 . A clamping circuit connects to a serial the MOS transistor which the source and the gate were made to short-circuit and was used as the

constant current load, and when the electrical-potential-difference value defined beforehand is supervised and the electrical-potential-difference value is exceeded with the number of the transistors which connect, it is made to output an STP signal. As shown in this drawing, in this example, two clamping circuits 17a and 17b and OR circuit 17c are constituted, and the rewriting electrical potential difference Vpp which a booster circuit 16 outputs is inputted into each clamping circuit 17a and 17b. a MOS transistors used as the constant current load are connected to one clamping circuit 17a, and it is the transistor T1 for control to the last stage. It is inserted and the SELR signal is inputted into the gate as a control signal. b MOS transistors used as the constant current load are connected to clamping circuit 17b of another side, and it is the transistor T2 for control to the last stage. It is inserted and the SELT signal is inputted into the gate as a control signal. And the output of each clamping circuit 17a and 17b is made as [output / through OR circuit 17c / as an STP signal]. That is, when the rewriting electrical potential difference to which clamping circuit 17a operates and is set when a SELR signal is outputted from the chip select buffer 15 is supervised, an STP signal is outputted and a SELT signal is outputted from the chip select buffer 15, it is constituted so that the rewriting electrical potential difference to which clamping circuit 17b operates and is set may be supervised and an STP signal may be outputted.

[0018] Drawing 4 is the detail drawing of the data-hold electrical-potential-difference creation circuit 18 shown in drawing 1 . It is transistor T3 as which the data-hold electrical-potential-difference creation circuit 18 inputted BI0 signal into the gate as shown in this drawing. The output control of the supply voltage Vcc is carried out. That is, it is transistor T3 when BI0 signal is outputted from the chip select buffer 15. It turns on and supply voltage Vcc is outputted. The supply voltage Vcc is made as [impress / at the control gate (CG) of each cel of the real cel 11 and a test cell 12].

[0019] Drawing 5 is the signal logic of E2 P-ROM of this example, and an explanatory view of operation. In E2 P-ROM of this example, if the burn-in cel 13 has writing through the burn-in cel write-in circuit 14 from the exterior as shown in drawing 1 , the burn-in cel 13 will emit a BIA signal, and will make the interior of equipment test mode. That is, as shown in drawing 5 , when the time of a BIA signal becoming logic"H" becomes test mode and the logic" chip select (CS) signal of H" is inputted as an access signal in this condition, the chip select buffer 15 turns ON a SELT signal. As only a test cell 12 will be chosen by this and access concerning the writing from the outside, elimination, and read-out was explained in drawing 2 , the cel of either of the test-cell array 12a is accessed, and real cel array 11a is not accessed. Moreover, in this condition, as shown in drawing 3 , the rewriting electrical potential difference pressure up is carried out [an electrical potential difference] in a booster circuit 16 by the monitor electrical potential difference set as clamping circuit 17b is decided, and when that rewriting electrical potential difference is writing or elimination, a test cell 12 is supplied.

[0020] And if CS signal is made into logic "L" when a BIA signal is logic"H", the chip select buffer 15 will turn ON BI0 signal. By this, the data-hold electrical-potential-difference creation circuit 18 will operate, and supply voltage Vcc will be impressed to the control gate of the real cel 11 and all the cels of a test cell 12.

[0021] If CS signal will be in the condition of standby of the real cel 11 by logic"H" and CS signal is made into logic "L" on the other hand when the burn-in cel 13 is eliminated and a BIA signal is made into logic "L", the chip select buffer 15 will turn ON a SELR signal. As only the real cel 11 was chosen by this and access concerning the writing from the outside, elimination, and read-out was explained in drawing 2 , the cel of either of the real cel array 11a is accessed, and test-cell array 12a is not accessed. Moreover, in this condition, as shown in drawing 3 , the rewriting electrical potential difference pressure up is carried out [an electrical potential difference] in a booster circuit 16 by the monitor electrical-potential-difference value set as clamping circuit 17b is decided, and when that rewriting electrical potential difference is writing or deletion, the real cel 11 is supplied.

[0022] Next, the property guarantee test of E2 P-ROM of this example is explained. Drawing 6 is a condition table at the time of usual [of E2 P-ROM of this example], and a trial. Clamping circuit 17a which showed E2 P-ROM in the conditions shown in this table to drawing 3 is set as the monitor electrical potential difference which is 25V for 20V and clamping circuit 17b, and Vcc of the data-hold electrical-potential-difference creation circuit 18 is set as 7V. A property guarantee test puts E2 P-ROM on the bottom of the temperature environment of 150-degreeC, and is performed about the count guarantee test of rewriting, and a data-hold guarantee test. A testing device 2 accesses the burn-in cel write-in circuit 14 of E2 P-ROM1 first, and writes in the burn-in cel 13, and the count guarantee test of rewriting makes a BIA signal "H", sets the inside of equipment as test mode, and then makes CS signal logic"H". And it eliminates by carrying out sequential access of each cel of a test cell 12, and writing in data. The writing of this data and elimination are repeated the number of predetermined times. Unlike 20V at the time, 25V are usually impressed for the electrical-potential-difference impression to the gate accompanying that write-in elimination, and data write-in elimination at this time is performed by giving stress severer than a real service condition. After the writing of the count of predetermined and elimination are completed, it writes in normally to each cel of a test cell 12, and it is

confirmed whether elimination is made or not. If normal, a data-hold guarantee test will be performed next. time amount neglect predetermined in the condition of the data-hold guarantee test having made CS signal logic "L", and having impressed 7V to the control gate of the real cel 11 and all the cels of a test cell 12, and having made data-hold into instability -- it carries out. Data are read after progress of predetermined time, collating with write-in data is performed, and maintenance of data is checked.

[0023] Thus, in this example, in the count guarantee test of rewriting, writing and elimination are performed on the still high tension electrical potential difference of 25V, rather than the electrical potential difference of 20V used for usual writing and usual elimination, since it becomes the trial which gives stress severer than a real service condition to a cel, a guarantee test can be attained by the count of rewriting smaller than before, and test time is shortened. Moreover, in a data-hold guarantee test, an electrical potential difference higher than the electrical potential difference usually impressed in the data-hold condition at the time at the control gate is impressed, since it becomes the trial of changing into the electrical-potential-difference condition that a data-hold condition becomes instability, a guarantee test can be attained by neglect time amount shorter than before, and test time is shortened.

[0024] Moreover, since the trial of this example is performed to E2 P-ROM by preparing the test cell which uses it only at the time of a test, it can carry out the trial to total and its dependability of a property guarantee improves.

[0025] Furthermore, since the burn-in cel which makes the interior of equipment test mode is prepared in E2 P-ROM of this example, while not creating a special electrical potential difference in the testing device and being in test mode, a special electrical potential difference did not need to be inputted into E2 P-ROM, and the burden of a testing device has been mitigated.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the outline block diagram of one example of E2 P-ROM of this invention.
[Drawing 2] It is a detailed circuit diagram about the selection of the real cel in an example, and a test cell.
[Drawing 3] It is the detailed circuit diagram of the clamping circuit of an example.
[Drawing 4] It is the detail drawing of the data-hold electrical-potential-difference creation circuit of an example.
[Drawing 5] It is the signal logic of E2 P-ROM and the explanatory view of operation in this example.
[Drawing 6] It is a condition table at the time of usual [of E2 P-ROM of this example], and a trial.
[Description of Notations]
1 -- E2 P-ROM
2 -- Testing device
11 -- Real cel
12 -- Test cell
13 -- Burn-in cel
14 -- Burn-in cel write-in circuit
15 -- Chip select buffer circuit
16 -- Booster circuit
17, 17a, 17b -- Clamping circuit
18 -- Data-hold electrical-potential-difference creation circuit
11a -- Real line array
12a -- Test line array
WL -- WORD line
BL -- Bit line
20, 20a, 20b -- Bit-line decoder

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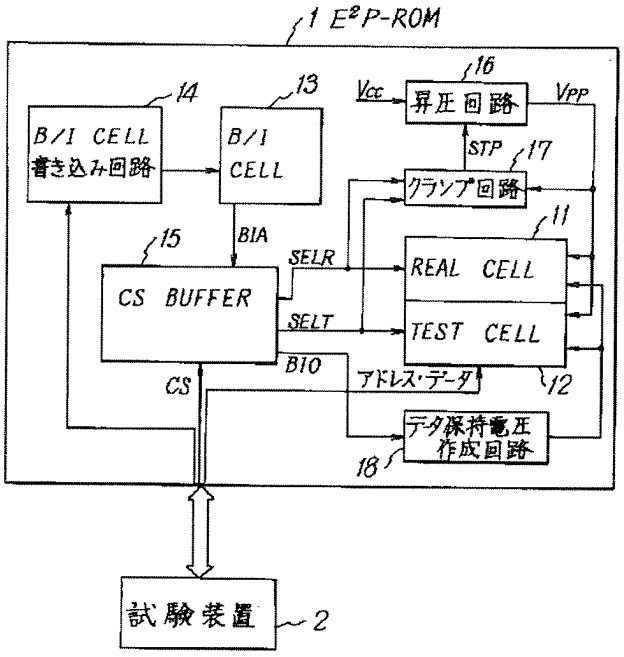
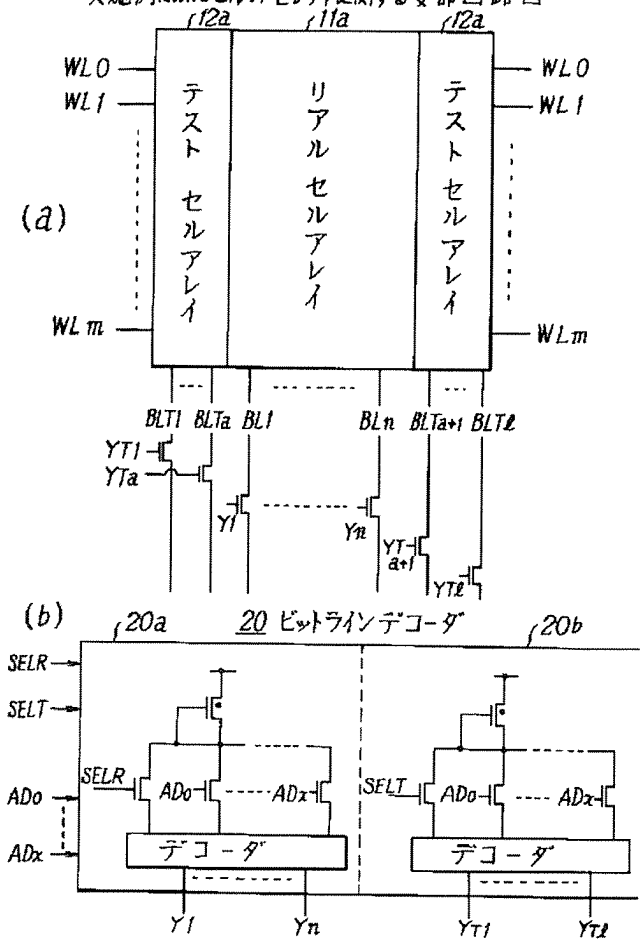
DRAWINGS

[Drawing 1]
本発明の一実施例の概略構成図



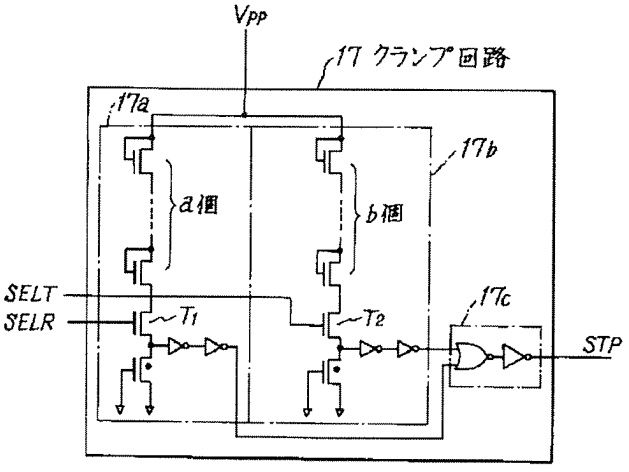
[Drawing 2]

実施例におけるセルのセレクトに関する要部回路図



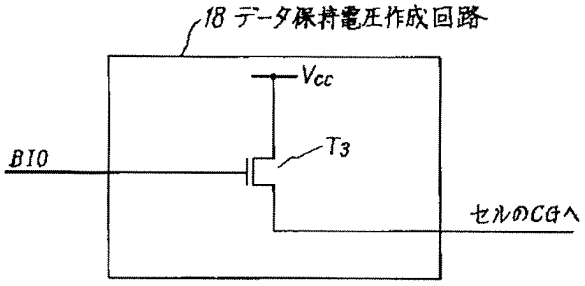
[Drawing 3]

本実施例のクランプ回路の詳細な回路図



[Drawing 4]

本実施例のデータ保持電圧作成回路の詳細図



[Drawing 5]
本実施例におけるE^2P-ROMの信号論理と動作の説明図

BIA信号	CS信号	動作
H	H	TEST CELL 選択 (SELT信号オン)
	L	TEST & REAL CELL 選択 (EEPROM CGにVcc) (BIO信号オン)
L	H	REAL CELL 選択 (スタンバイ)
	L	REAL CELL 選択 (アクティブ) (SELR信号オン)

[Drawing 6]
実施例の通常時と試験時の条件表

	通常時	試験時
書込み消去電圧 (VPP)	～20V	～25V
データ保持の時のコントロールゲート電圧	0～2V	～7V
温度環境	0～70°C	150°C

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] In the non-volatile semiconductor memory with which the writing and elimination of data are made electrically The burn-in cel holding the mode condition which switched the inside of equipment to the normal mode and test mode, and was switched by setting out from the outside (13), The real cel in which access is made only at the time of said normal mode (11), The test cell by which access is made only at the time of said test mode (12), The rewriting electrical-potential-difference pressure-up means which makes the writing of data, or the electrical potential difference for elimination higher than the time of the normal mode at the time of said test mode (16 17), The non-volatile semiconductor memory characterized by having a CG electrical-potential-difference pressure-up means (18) to impress an electrical potential difference higher than the time of the normal mode to the control gate of a cel when there is no access at the time of said test mode.
[Claim 2] Are the test method of a non-volatile semiconductor memory according to claim 1, put said non-volatile semiconductor memory on the bottom of hot environments, and said burn-in cel (13) is set as test mode. Said rewriting electrical-potential-difference pressure-up means (16 17) is made to perform the writing and elimination of the data to said test cell (12) on an electrical potential difference higher than the time of the normal mode. The test method of the non-volatile semiconductor memory which writes in the writing of the data to said test cell (12), and access of elimination after the count repeat of predetermined, and its access termination, and is characterized by what is judged by performing read-out of data and collating.
[Claim 3] Are the test method of a non-volatile semiconductor memory according to claim 1, put said non-volatile semiconductor memory on the bottom of hot environments, and said burn-in cel (13) is set as the normal mode. Write predetermined data in said real cel (11), next said burn-in cel (13) is set as test mode. Without writing predetermined data in said test cell (12), and performing access after that, where an electrical potential difference higher than the time of the normal mode is impressed to the control gate of a cel by said CG electrical-potential-difference pressure-up means (18) The test method of the non-volatile semiconductor memory which carries out predetermined time neglect and is characterized by what it writes in from said test cell (12) and real cel (11) after the predetermined time progress, data are read, and is collated and judged.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] Since it is considering as the property guarantee test accelerated more in time by adding stress severer than a real service condition to a cel inside in this invention as explained above, the effectiveness of shortening test time is size. Moreover, since a 100% test becomes possible by having prepared the test cell, dependability can be raised.

[Translation done.]